What Is Claimed Is:

1. A method for manufacturing a semiconductor device in which a plurality of semiconductor layers are sequentially formed over a semiconductor substrate in a laminating manner, a hetero junction bipolar transistor, a Schottky diode and a resistance element are formed in a monolithic manner, and an isolation for establishing an electric insulation is provided at least between the hetero junction bipolar transistor and the Schottky diode, wherein respective semiconductor layers which are formed into a sub collector layer, a collector layer, a base layer, a wide gap emitter layer and an emitter layer are sequentially formed over one surface of the semiconductor substrate, and thereafter, in the manufacture of the hetero junction bipolar transistor, among the respective semiconductor layers, the given semiconductor layers are formed in given patterns by sequential etching thus sequentially forming an emitter layer, a wide gap emitter layer, the base layer, the collector layer and the sub collector layer, and at the same time, an emitter electrode is formed over the emitter layer, an alloying treatment is applied to the wide gap emitter layer which extends around the emitter layer thus forming a base electrode which is

electrically connected to the base layer, and a collector electrode is formed over the collector layer which extends around the base layer thus forming the hetero junction bipolar transistor,

wherein, in the manufacture of the Schottky diode, a Schottky electrode is formed over a semiconductor layer corresponding to the collector layer, and an ohmic electrode for diode is formed over a semiconductor layer corresponding to the sub collector layer thus forming the Schottky diode,

wherein, in the manufacture of the resistance element, a resistance film is formed over an insulation film in a region outside a region where the hetero junction bipolar transistor and the Schottky diode are formed thus forming the resistance element, and

wherein the Schottky electrode and the resistance film are simultaneously formed using a same material.

2. A method for manufacturing a semiconductor device according to claim 1, wherein the Schottky electrode and the base electrode are different layers which are not formed simultaneously.

3. A method for manufacturing a semiconductor device according to claim 1, wherein the base electrode is formed

such that the base electrode surrounds the emitter layer and, at the same time, a region ranging from the base electrode to the inside of the base electrode except for an outer periphery of the base electrode is covered with a mask for etching, and the collector layer is etched to an intermediate depth thereof using the mask for etching and the base electrode as masks thus forming the mesa-shaped base layer.

4. A method for manufacturing a semiconductor device according to claim 1,

wherein an etching stopper layer which is formed of a material having an etching speed lower than an etching speed of the sub collector layer is formed between the semiconductor substrate and the sub collector layer and,

wherein the formation of the separation groove which is served for establishing the electric insulation of the hetero junction bipolar transistor and reaches a surface layer of the semiconductor substrate from the sub collector layer includes an etching treatment in which etching of the sub collector layer is stopped at the etching stopper layer, an etching treatment in which the etching stopper layer is etched, and an etching treatment in which a surface layer portion of the semiconductor substrate is etched.

5. A method for manufacturing a semiconductor device according to claim 1,

wherein an etching stopper layer which is formed of a material having an etching speed lower than an etching speed of the collector layer is formed between the sub collector layer and the collector layer, and

wherein, in etching which is performed to expose the sub collector layer by etching the collector layer, the etching is stopped at the etching stopper layer.

6. A method for manufacturing a semiconductor device according to claim 1, wherein the semiconductor substrate is formed of a semi-insulating GaAs substrate, the sub collector layer is formed of a first conductive-type GaAs layer, the collector layer is formed of a first conductive-type GaAs layer, the base layer is formed of a second conductive-type GaAs layer, the wide gap emitter layer is formed of a first conductive-type InGaP layer, and the emitter layer is formed of a first conductive type GaAs layer having an InGaAs layer as a surface layer thereof.

7. A method for manufacturing a semiconductor device according to claim 6, wherein the etching stopper layer is formed of a first conductive InGaP layer.

8. A method for manufacturing a semiconductor device according to claim 1, wherein the Schottky electrode and the resistance film are made of alloy which mainly contains a high melting-point material or silicide and have given portions to which lines made of aluminum are overlapped.

9. A method for manufacturing a semiconductor device,

wherein respective semiconductor layers which are formed into a sub collector layer, a collector layer, a mesa-shaped base layer, a wide gap emitter layer and an emitter layer are sequentially formed over one surface of a semiconductor substrate,

wherein an isolation which establishes an electric insulation is formed between a region in which a hetero junction bipolar transistor is formed and other elements,

wherein, in the region in which the hetero junction bipolar transistor is formed, among the respective semiconductor layers, the given semiconductor layers are formed in given patterns by sequential etching thus sequentially forming an emitter layer, a wide gap emitter

layer, the mesa-shaped base layer, the collector layer and the sub collector layer,

wherein an emitter electrode is formed over the emitter layer,

wherein an alloying treatment is applied to the wide gap emitter layer which extends around the emitter layer to form a base electrode which is electrically connected to the base layer, and

wherein a collector electrode is formed over a collector layer which extends around the base layer so as to manufacture the hetero junction bipolar transistor, and

wherein the mesa-shaped base layer is formed after forming the base electrode.

10. A method for manufacturing a semiconductor device according to claim 9, wherein the base electrode is formed such that the base electrode surrounds the emitter layer and, at the same time, a region ranging from the base electrode to the inside of the base electrode except for an outer periphery of the base electrode is covered with a mask for etching, and the collector layer is etched to an intermediate depth thereof using the mask for etching and the base electrodes as masks thus forming the mesa-shaped base layer.

11. A method for manufacturing a semiconductor device according to claim 9, wherein an etching stopper layer which is formed of a material having an etching speed lower than an etching speed of the sub collector layer is formed between the semiconductor substrate and the sub collector layer and, at the same time, an etching stopper layer which is formed of a material having an etching speed lower than an etching speed of the collector layer is formed between the sub collector layer and the collector layer,

wherein etching which is performed to expose the sub collector layer by etching the collector layer is completed by stopping the etching at the etching stopper layer, and

wherein the formation of a separation groove for the isolation includes an etching treatment in which etching of the sub collector layer is stopped at the etching stopper layer, an etching treatment in which the etching stopper layer is etched, and an etching treatment in which a surface layer portion of the semiconductor substrate is etched.

12. A method for manufacturing a semiconductor device according to claim 9, wherein the semiconductor substrate is formed of a semi-insulating GaAs substrate, the sub collector layer is formed of a first conductive-type GaAs layer, the collector layer is formed of a first conductive-

type GaAs layer, the base layer is formed of a second conductive-type GaAs layer, the wide gap emitter layer is formed of a first conductive-type InGaP layer, the emitter layer is formed of a first conductive type GaAs layer having an InGaAs layer as a surface layer thereof, and the etching stopper layer is formed of a first conductive-type InGaP layer.

13. A method for manufacturing a semiconductor device in which a plurality of semiconductor layers are sequentially formed over a semiconductor substrate in a laminating manner, a hetero junction bipolar transistor, a Schottky diode and a resistance element are formed in a monolithic manner, and an isolation for establishing an electric insulation is provided at least between the hetero junction bipolar transistor and the Schottky diode,

wherein respective semiconductor layers which are formed into a sub collector layer, a collector layer, a base layer, a wide gap emitter layer and an emitter layer are sequentially formed over one surface of the semiconductor substrate, and thereafter, in the manufacture of the hetero junction bipolar transistor, among the respective semiconductor layers, the given semiconductor layers are formed in given patterns by sequential etching thus

sequentially forming an emitter layer, a wide gap emitter layer, the base layer, the collector layer and the sub collector layer, and at the same time, an emitter electrode is formed over the emitter layer, an alloying treatment is applied to the wide gap emitter layer which extends around the emitter layer thus forming a base electrode which is electrically connected to the base layer, and a collector electrode is formed over the collector layer which extends around the base layer thus forming the hetero junction bipolar transistor,

wherein, in the manufacture of the Schottky diode, a Schottky electrode is formed over a semiconductor layer corresponding to the collector layer, and an ohmic electrode for diode is formed over a semiconductor layer corresponding to the sub collector layer thus forming the Schottky diode,

wherein, in the manufacture of the resistance element, a resistance film is formed over an insulation film in a region outside a region where the hetero junction bipolar transistor and the Schottky diode are formed thus forming the resistance element, and

wherein the emitter electrode and the resistance film are simultaneously formed using a same material.

14. A method for manufacturing a semiconductor device according to claim 13, wherein the base electrode is formed such that the base electrode surrounds the emitter layer and, at the same time, a region ranging from the base electrode to the inside of the base electrode except for an outer periphery of the base electrode is covered with a mask for etching, and the collector layer is etched to an intermediate depth thereof using the mask for etching and the base electrodes as masks thus forming the mesa-shaped base layer.

15. A method for manufacturing a semiconductor device according to claim 13, wherein the emitter electrode and the resistance film are made of alloy which mainly contains a high melting-point metal material or silicide and have given portions on which lines made of aluminum are overlapped.

16. A method for manufacturing a semiconductor device according to claim 13, wherein an etching stopper layer which is formed of a material having an etching speed lower than an etching speed of the sub collector layer is formed between the semiconductor substrate and the sub collector layer and, at the same time, an etching stopper layer which is formed of a material having an etching speed lower than

an etching speed of the collector layer is formed between the sub collector layer and the collector layer,

wherein an etching which is performed to expose the sub collector layer by etching the collector layer is completed by stopping the etching at the etching stopper layer, and

wherein the formation of a separation groove for isolation includes an etching treatment in which etching of the sub collector layer is stopped at the etching stopper layer, an etching treatment in which the etching stopper layer is etched, and an etching treatment in which a surface layer portion of the semiconductor substrate is etched.

17. A method for manufacturing a semiconductor device according to claim 16, wherein the semiconductor substrate is formed of a semi-insulating GaAs substrate, the sub collector layer is formed of a first conductive-type GaAs layer, the collector layer is formed of a first conductive-type GaAs layer, the base layer is formed of a second conductive-type GaAs layer, the wide gap emitter layer is formed of a first conductive-type InGaP layer, the emitter layer is formed of a first conductive type GaAs layer having an InGaAs layer as a surface layer thereof, and the etching stopper layer is formed of a first conductive-type InGaP layer.

18. A method for manufacturing a semiconductor device in which a plurality of semiconductor layers are sequentially formed over a semiconductor substrate in a laminating manner, a hetero junction bipolar transistor, a Schottky diode and a resistance element are formed in a monolithic manner, and an isolation for establishing an electric insulation is provided at least between the hetero junction bipolar transistor and the Schottky diode,

wherein respective semiconductor layers which are formed into a sub collector layer, a collector layer, a base layer, a wide gap emitter layer and an emitter layer are sequentially formed over one surface of the semiconductor substrate, and thereafter, in the manufacture of the hetero junction bipolar transistor, among the respective semiconductor layers, the given semiconductor layers are formed in given patterns by sequential etching thus sequentially forming an emitter layer, a wide gap emitter layer, the base layer, the collector layer and the sub collector layer, and at the same time, an emitter electrode is formed over the emitter layer, an alloying treatment is applied to the wide gap emitter layer which extends around the emitter layer thus forming a base electrode which is electrically connected to the base layer, and a collector

electrode is formed over the collector layer which extends around the base layer thus forming the hetero junction bipolar transistor,

wherein, in the manufacture of the Schottky diode, a Schottky electrode is formed over a semiconductor layer corresponding to the collector layer, and an ohmic electrode for diode is formed over a semiconductor layer corresponding to the sub collector layer thus forming the Schottky diode,

wherein, in the manufacture of the resistance element, a resistance film is formed over an insulation film in a region outside a region where the hetero junction bipolar transistor and the Schottky diode are formed thus forming the resistance element, and

wherein the emitter electrode, the Schottky electrode and the resistance film are simultaneously formed using a same material.

19. A method for manufacturing a semiconductor device according to claim 18, wherein the base electrode is formed such that the base electrode surrounds the emitter layer and, at the same time, a region ranging from the base electrode to the inside of the base electrode except for an outer periphery of the base electrode is covered with a mask for etching, and the collector layer is etched to an

intermediate depth thereof using the mask for etching and the base electrodes as masks thus forming the mesa-shaped base layer.

20. A method for manufacturing a semiconductor device according to claim 18, wherein the emitter electrode, the Schottky electrode and the resistance film are made of alloy which mainly contains a high melting-point material or a silicide and have given portions on which lines made of aluminum are overlapped.

21. A method for manufacturing a semiconductor device according to claim 18, wherein an etching stopper layer which is formed of a material having an etching speed lower than an etching speed of the sub collector layer is formed between the semiconductor substrate and the sub collector layer and, at the same time, an etching stopper layer which is formed of a material having an etching speed lower than an etching speed of the collector layer is formed between the sub collector layer and the collector layer,

wherein an etching which is performed to expose the sub collector layer by etching the collector layer is completed by stopping the etching at the etching stopper layer, and

wherein the formation of a separation groove for the isolation includes an etching treatment in which etching of the sub collector layer is stopped at the etching stopper layer, an etching treatment in which the etching stopper layer is etched, and an etching treatment in which a surface layer portion of the semiconductor substrate is etched.

22. A method for manufacturing a semiconductor device according to claim 21, wherein the semiconductor substrate is formed of a semi-insulating GaAs substrate, the sub collector layer is formed of a first conductive-type GaAs layer, the collector layer is formed of a first conductive-type GaAs layer, the base layer is formed of a second conductive-type GaAs layer, the wide gap emitter layer is formed of a first conductive-type InGaP layer, the emitter layer is formed of a first conductive type GaAs layer having an InGaAs layer as a surface layer thereof, and the etching stopper layer is formed of a first conductive-type InGaP layer.

23. A method for manufacturing a semiconductor device comprising

a semiconductor substrate,

a plurality of semiconductor layers which are sequentially formed in an overlapped manner on one surface of the semiconductor substrate, and

a plurality of circuit elements which are formed over the semiconductor substrate and the semiconductor layers,

wherein one or the plurality of circuit elements are formed electrically independently from each other by being surrounded by a separation groove which reaches a surface layer of the semiconductor substrate from the semiconductor layer, and the given circuits elements are electrically connected to each other by lines which extend and traverse the separation groove, and

the method comprising the steps of:

forming, between the semiconductor substrate and the semiconductor layer which is formed as a layer above the semiconductor substrate, an etching stopper layer which is formed of a material having an etching speed lower than an etching speed of the semiconductor layer which is formed as a layer above the semiconductor substrate, and

forming the separation groove by including an etching treatment in which etching of the semiconductor layer which is formed as a layer above the etching stopper layer is stopped at the etching stopper layer, an etching treatment in which the etching stopper layer is etched, and an etching

treatment in which a surface layer portion of the semiconductor substrate is etched.

24. A method for manufacturing a semiconductor device according to claim 23, comprising the steps of:

sequentially forming, over one surface of a semiconductor substrate, respective semiconductor layers which into a sub collector layer, a collector layer, a base layer, a wide gap emitter layer and an emitter layer,

among the respective semiconductor layers, forming the given semiconductor layers in given patterns by sequential etching thus sequentially forming the emitter layer, the wide gap emitter layer, the base layer, the collector layer and the sub collector layer,

forming an emitter electrode over the emitter layer,

applying an alloying treatment to the wide gap emitter layer which extends around the emitter layer to form a base electrode which is electrically connected to the base layer, and

forming a collector electrode over a collector layer which extends around the base layer so as to manufacture the hetero junction bipolar transistor.

25. A method for manufacturing a semiconductor device according to claim 24, wherein an etching stopper layer which is formed of a material having an etching speed lower than an etching speed of the collector layer is formed between the sub collector layer and the collector layer, and

wherein, in an etching which is performed to expose the sub collector by etching the collector layer, the etching is stopped at the etching stopper layer.

26. A method for manufacturing a semiconductor device according to claim 25, wherein the semiconductor substrate is formed of a semi-insulating GaAs substrate, the sub collector layer is formed of a first conductive-type GaAs layer, the collector layer is formed of a first conductive-type GaAs layer, the base layer is formed of a second conductive-type GaAs layer, the wide gap emitter layer is formed of a first conductive-type InGaP layer, the emitter layer is formed of a first conductive type GaAs layer having an InGaAs layer as a surface layer thereof, and the etching stopper layer is formed of a first conductive type InGap layer.

27. A method for manufacturing a semiconductor device according to claim 26, wherein a thickness of the etching

stopper layer which is formed of the InGaP is set to approximately several tens nm which does not generate a grid misalignment between the InGaP layer and the GaAs layer.

28. A method for manufacturing a semiconductor device having a bipolar transistor, a Schottky diode, and a resistance element formed in a first region, a second region, and a third region of a semiconductor substrate, respectively, said method comprising the steps of:

(a) forming the bipolar transistor in the first region;

(b) forming a first semiconductor layer of the Schottky diode in the second region;

(c) forming an ohmic electrode of the Schottky diode, electrically connected to the first semiconductor layer, in the second region; and

(d) forming a Schottky electrode of the Schottky diode, electrically connected to the first semiconductor layer, in the second region and a resistance film of the resistance element in the third region;

wherein in the step (d), the Schottky electrode and the resistance film are made of a same layer.

29. A method according to Claim 28, wherein in the step (d), the Schottky electrode and the resistance film are simultaneously formed.

30. A method according to Claim 28, wherein the bipolar transistor is a hetero-junction bipolar transistor.

31. A method according to Claim 30, wherein the semiconductor substrate is made of GaAs.

32. A method according to Claim 31, wherein the Schottky electrode and the resistance film are made of WSiN.

33. A method for manufacturing a semiconductor device having a bipolar transistor, a Schottky diode, and a resistance element formed in a first region, a second region, and a third region of a semiconductor substrate, respectively, said method comprising the steps of:

(a) forming an emitter layer of the bipolar transistor in the first region;

(b) forming a base layer of the bipolar transistor, under the emitter layer, in the first region;

(c) forming a collector layer of the bipolar transistor, under the base layer, in the first region, and a

first semiconductor layer of the Schottky diode in the second region;

(d) forming an ohmic electrode of the Schottky diode, electrically connected to the first semiconductor layer, in the second region; and

(e) forming a Schottky electrode of the Schottky diode, electrically connected to the first semiconductor layer, in the second region, and a resistance film of the resistance element in the third region;

wherein in the step (e), the Schottky electrode and the resistance film are made of a same layer.

34. A method according to Claim 33, wherein the first semiconductor layer of the Schottky diode and the collector layer are made of a same layer.

35. A method according to Claim 34, wherein a separation groove is formed between the first region and the second region.

36. A method according Claim 35, wherein the bipolar transistor is a hetero-junction bipolar transistor, and the semiconductor substrate is made of GaAs.

37. A method according to Claim 33, further comprising the step of:

(f) forming a first wiring electrically connected to the emitter layer, a second wiring electrically connected to the base layer, a third wiring electrically connected to the collector layer, a fourth wiring electrically connected to the ohmic electrode, a fifth wiring electrically connected to the Schottky electrode, a sixth wiring electrically connected to the resistance film, and a seventh wiring electrically connected to the resistance film;

wherein the fifth to seventh wirings are made of a same material.